A Folded Voltage-Combiners Biased Amplifier for Low Voltage and High Energy-Efficiency Applications

Ricardo Póvoa, Nuno Lourenço, Ricardo Martins, António Canelas, Nuno Horta, and João Goes

***Abstract*—The topic of this brief is a single-stage amplifier biased by a doublet of voltage-combiners in a folded configuration, in order to be supplied by a power source of 1.2 V, maintaining proper dc biasing and avoiding the need of any device stacking. The topology has been automatically designed, optimized, and laid out, from sizing to layout level, using a layout-aware approach provided by the AIDA framework, a state-of-the-art analog IC design optimization framework. Experimental results prove that a gain of approximately 44 dB, together with a figure-of-merit higher than 1300 MHz × pF/mW are achievable using the proposed topology, with standard UMC 130 nm technology devices and a 1.2-V supply source. Finally, an extension to supply sources below nominal is explored, showing exciting results toward a future of high energy-efficiency amplifiers.**

***Index Terms*—Folded voltage-combiners, single-stage, OTA, low-power, low-voltage, energy-efficiency, gain improvement.**

I. Introduction

THE REQUIREMENTS of power reduction in electronic circuitry, visible in both professional and personal applications of the everyday life, together with the late trend of modern complementary metal-oxide-semiconductor (CMOS) technologies to use lower supply voltages, drives the evermore challenging design of amplifiers [1]. The latter, in general, follows the straightforward concept of multiple cascaded gain stages, since the classic cascode approach suffers from output-swing (OS) reduction, due to transistor stacking, increasing the complexity of the circuits, hence, their production cost. Reducing power in analog circuitry is directly associated with the energy-efficiency of the amplifiers. Therefore, the need for high performance together with high energy-efficiency urges in the particular design of amplifiers [2]. In these terms, new and improved topologies have to be developed and proposed, with energy-efficiency under concern.

Manuscript received February 22, 2019; accepted April 19, 2019. Date of publication April 24, 2019; date of current version January 31, 2020. This work was supported in part by the Fundação para a Ciência e Tecnologia under Grant SFRH/BD/103337/2014, Grant SFRH/BPD/104648/2014, and Grant SFRH/BPD/120009/2016, and in part by the Instituto de Telecomunicações under Project UID/EEA/50008/2019. This brief was recommended by Associate Editor H. Shibata. *(Corresponding author: Ricardo Póvoa.)*

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Digital Object Identifier 10.1109/TCSII.2019.2913083

In the extensive context of the Internet-of-things (IOT), with grand emphasis and impact in modern wireless telecommunications, analog amplifiers play a most significant role, and, particularly, the energy-efficiency is of major importance [3]–[5]. In parallel, the concern over gain improvement strategies is of highest importance, simply due to the fact that designs targeting deeper nanoscale technologies suffer a decrease in terms of the intrinsic gain of the devices, i.e., *gm*/*gds* where *gm* and *gds* represent respectively the main transconductance and the output conductance of the devices, to an estimate value smaller than 20 dB, i.e., 10 V/V, while the variability of the intrinsic gain may be in the range of ± 10 dB [2]. This brief addresses these two matters. The necessity for energy-efficiency and the progress of gain improvement strategies, free from cascode implementations, and following the tendency of lower voltage supplies, by proposing the final step towards a complete new family of single-stage amplifier topologies, to be implemented as a stand-alone or as part of multi-stage amplifier chains in the nowadays intensifying standpoint of IOT [6], [7]. This brief proposes an operational transconductance amplifier (OTA) biased by a doublet of folded voltage-combiners, designed to operate with a nominal voltage supply source spanning from 1.2V down to 0.9 V, without any stacking issues, maintaining proper DC biasing, compounded by low systematic offset and maximum OS. The proposed topology derives from the symmetrical CMOS OTA, yet with the replacement of the differential-pair biasing current source by a fully-differential folded voltage-combiner (VC) circuit. This circuit has a differential input combined with folded common-drain (CD) and common-source (CS) devices. This topology, when connected in this way, delivers a double effect: the fully-differential folded VC circuit increases the overall gain of the OTA, while the differential-pair transistors operate as CS and common-gate (CG) transistors, at the same time, yielding the exact same cascode behavior. When compared to the woks presented in [6] and [7], the implementation using low-voltage devices and the intrinsic biasing strategy of the folded VC circuit allow a reduced current draining with proper DC operating point establishment, which otherwise would not be possible for lower supply voltages, e.g., below 1.8 V. The OTA proposed in this brief is implemented using the UMC 130 nm CMOS technology design kit, and is automatically designed and optimized using AIDA-L, from sizing to layout, validated by XRC, i.e., extracted layout, simulations and experimental results, showing that a figure-of-merit (FOM) in the order of 1300 MHz×pF/mW together with a low-frequency gain higher than 40 dB are reachable with this topology, with strong reliability and accuracy throughout.

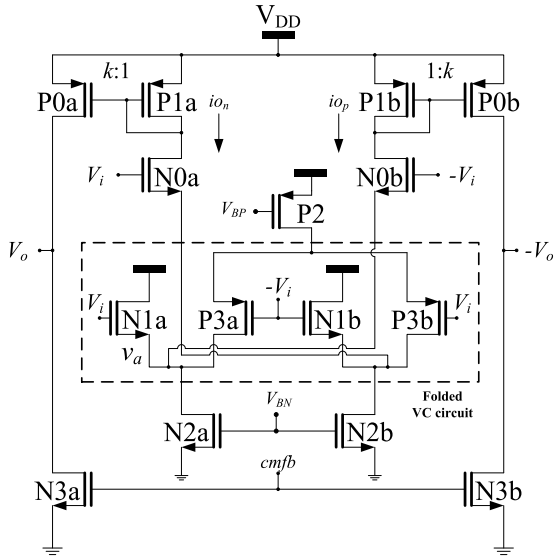

Fig. 1. Electrical scheme of the proposed folded VC biased OTA.

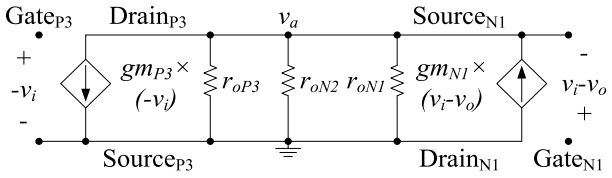

Fig. 2. Fully-differential folded VC small-signal equivalent circuit.

This brief is structured as follows: Section II presents an analytical and circuit description of the proposed OTA topology; Section III presents the details of the circuit optimization framework and design setup; Section IV presents XRC simulation and experimental results, with the positioning among other single-stage amplifiers published in recent literature and further simulation-level verifications for power supplies below 1.2 V and, finally, Section V draws the conclusions.

II. Topological Description

The suggested response to lower voltage supplies relies on a topology in which the static current source that bias the differential-pair is substituted by a fully-differential folded voltage-combiner circuit, i.e., a differential input combined with folded CD and CS devices, as it is described further. The electrical scheme of a fully-differential folded VC is highlighted inside Fig. 1, which illustrates the proposed OTA. The circuit employs two PMOS devices in a CS configuration, i.e., P3a and P3b, and two folded NMOS devices in a CD configuration, i.e., N1a and N1b, combined with a differential input, while being properly biased by the P2, N2a and N2b current sources. It is possible to determine the small-signal small-signal equivalent circuit of this circuit, as shown in Fig. 2, where the body-effectbody-effect of both N1 and P3 is not considered for simplicity. The gaingain of the fully-differential folded voltage-combiners circuit, A_{vVC}, is given by (1), neglecting the body-effect of N1 and P3. Considering that gm_{P3} and $gm_{N1} >> (gds_{N1} + gds_{P3} + gds_{N2})$ is a fair approximation of the gain in (1), the expression can be further simplified into (2). Comparing a basic CD, i.e., source-follower, with the folded VC, the advantage of the latter is clear: the gain can be made higher, by properly choosing $gm_{P3} > gm_{N1}$. The GBW is given by (3) and the thermal input-referred noise of the folded VC, considering the drain-source contributions exclusively, can be given by (4). Employing the described folded VC, in replacement of a conventional static basic current source that usually bias a differential-pair, in classic single-stage current-mirror OTAs, yields the proposed simplified OTA topology, shown in Fig. 3. Following simple circuit analysis, i.e., using Kirchhoffs' laws, and after resolving (5), the low-frequency gain of the amplifier, A_{vOTA}, can be described by (6), where k represents the mirroring factor, and gds_{out} is the output conductance, dependent on P0 and N3 devices. At this point, consider the inexistence of cascode devices stacked in the outer branches, hence maximizing the OS of the amplifier. Finally, this biasing strategy, with the implementation of low-voltage devices, ensures a smaller current drain for proper voltage operating point establishment, when compared to [6] and [7].

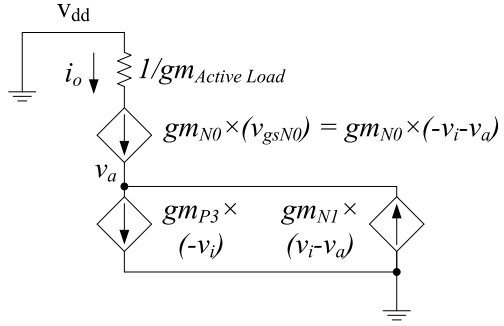

Fig. 3. Simplified folded VC biased OTA small-signal equivalent circuit.

$$A_{vVC} = \frac{gm_{N1} + gm_{P3}}{gm_{N1} + gds_{N1} + gds_{N2} + gds_{P3}} \tag{1}$$

$$A_{vVC} \approx 1 + \frac{gm_{P3}}{gm_{N1}} \Rightarrow \left|A_{vVC}\right| > 1 \tag{2}$$

$$\text{GBW} = \frac{gm_{N1} + gm_{P3}}{cdb_{P3} + cgd_{P3} + cgs_{N1} + cgd_{N2} + cdb_{N2}} \tag{3}$$

$$\overline{V^2_{n_{in_{P3}}}} = \frac{4kT\gamma gm_{N1} + 4kT\gamma gm_{P3} + 4kT\gamma gm_{N2}}{gm^2_{P3}} \tag{4}$$

$$-v_o = \frac{k \times gm_{N0} \times \left(-v_i - \left(v_i \times A_{vVC}\right)\right)}{gds_{P0} + gds_{N3}} \tag{5}$$

$$A_{vOTA} \approx \frac{k \times io}{gds_{P0} + gds_{N3}} = \frac{k \times gm_{N0} \times (1 + A_{vVC})}{gds_{OUT}}. \tag{6}$$

III. Optimization Framework and Design Setup

In order to obtain the best performance design solutions, and completely explore the tradeoffs between the low-frequency gain and the energy-efficiency FOM, in the design of the OTA proposed in this brief, a multi-objective and multi-constraint circuit optimization framework denominated AIDA - Analog IC Design Automation is utilized to automatically optimize the circuit at both sizing and layout levels [8], in what is denominated as layout-aware optimization. The optimization framework AIDA has an evolutionary computation kernel, and implements an automatic synthesis flow, where the circuit performance is evaluated in commercial electrical simulators. AIDA delivers a Pareto optimal front (POF) of feasible circuit solutions, i.e., a set of sized and laid out circuits,

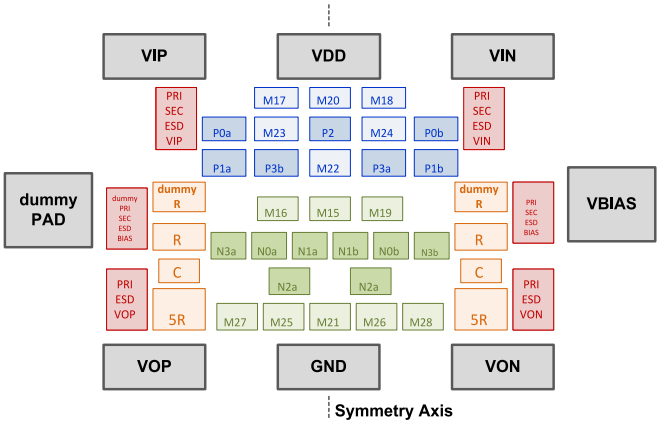

Fig. 4. Floorplan for the folded VC biased OTA used in AIDA-L.

TABLE I
FUNCTIONAL AND PERFORMANCE CONSTRAINTS FOR OPTIMIZATION

V_{DS}-VDS_{SAT}	≥ 50 mV	**GBW**	≥ 30 MHz
V_{GS}-V_T	≥ 50 mV	**Gain**	≥ 40 dB
Systematic Offset	≤ 1 mV	I_{DD}	≤ 2 mA
Width *per* Finger	≥ 720 nm	**PM**	≥ 50 °
Active Area *per* Device	≥ 1μm^2	**FOM**	≥ 750 MHz×pF/mW

all meeting the specifications, yet expressing the different compromises between the setup optimization objectives, this way providing the largest insight of the circuit under optimization. The AIDA framework is mainly composed of two modules: a sizing optimization module, i.e., AIDA-C [9], and an automatic layout generation module, i.e., AIDA-L [10]. The latter includes layout data, e.g., geometric and parasitic, in the sizing optimization flow. Also, AIDA-L, takes the device sizes and a floorplan provided by the designer, for the selected circuit sizing, and generates the complete layout by placing and routing the devices automatically. The floorplan used in this brief is shown in Fig. 4.

The design flow of AIDA-L is generally technology-independent, which means that the setup can be effortlessly recycled, either for different specifications or for different technological nodes. The most relevant and inconvenient issue is when the circuit topologies, for which the setup is defined, cannot fulfill the desired performance. In this situation, a variant of the previously defined topology needs to be implemented, if the constraints are still to be fully met. Nevertheless, most of the setup, e.g., test benches, metrics or high level floorplans, still hold, while AIDA can also import settings between projects with diverse setups, matching the previous aspects, e.g., ranges of the design variables, design objectives or performance and functional constraints, leaving only the new design variables and performance metrics to be user-defined. Finally, in order to translate the setup from one technology node to another, the only important changes to take into account are the models and the corresponding voltage supply values, considering that the topology and the measures are the same and, particularly in new technologies, the ranges of the variables differ, with clear modifications in the desired specifications.

The optimization process considers the maximization of the FOM given in (7), together with a maximization of the low-frequency gain of the OTA. Moreover, a complete set of performance and functional specifications are covered, as detailed in Table I. Looking towards physical implementation,

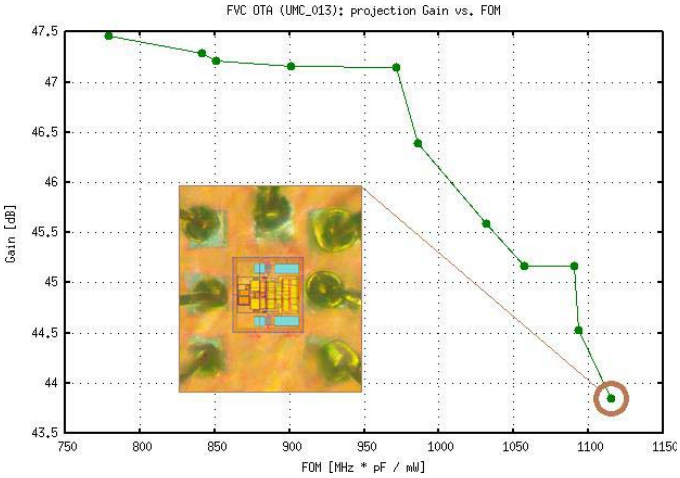

Fig. 5. POF: 4000 generations in typical and 1500 generations in corners.

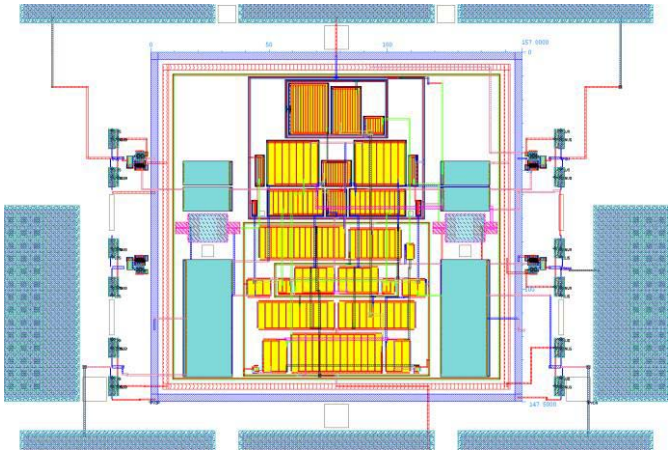

Fig. 6. Automatically generated layout: core with ∼ 157 μm ×147.5 μm.

minimum active areas and finger widths values are imposed, with a systematic offset of less than 1 mV, i.e., less than 0.1 % of the 1.2 V voltage supply source. The optimized design variables, are the finger lengths, widths and the number of fingers of all the active devices inside the circuit, including the common-mode circuitry. The optimization process takes into consideration corner case conditions, i.e., Fast-N/Fast-P, Fast-N/Slow-P, Slow-N/Fast-P and Slow-N/Slow-P device models, directly taken from the UMC 130 nm design kit.

$$\text{FOM} = \text{GBW} \times C_L/P_{DC}\big[\text{MHz} \times \text{pF/mW}\big] \tag{7}$$

IV. Optimized Designs and Post-Layout Results

The output of AIDA, shown in Fig. 5, presents completely laid out solutions with FOMs between 1115.6 and 778.8 MHz × pF/mW, all meeting the specifications shown in Table I. The layout core of the highlighted solution is shown in Fig. 6, with an approximated area of 0.023 mm^2. The insertion of dummy structures, e.g., left pad and electrostatic discharge protections ensure complete symmetry of the designed layout. Yet, they are not connected to the circuit core and can still be deleted before the final submission for fabrication. The circuit microphotograph is shown in Fig. 5, with superimposed layout due to the opaque passivation layer. The XRC simulation results, in typical voltage and temperature conditions,

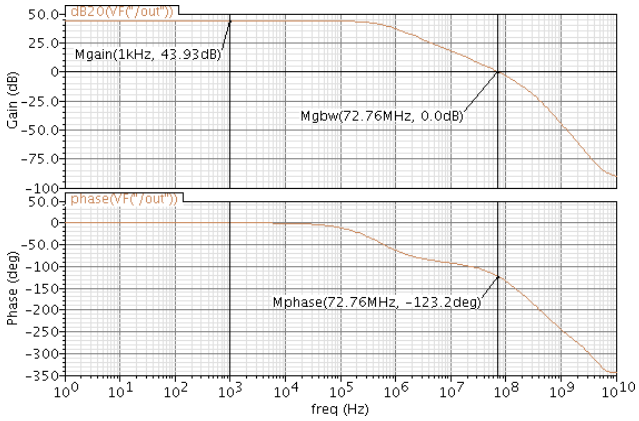

Fig. 7. AC response: Gain of 44 dB; Phase Margin of 57°.

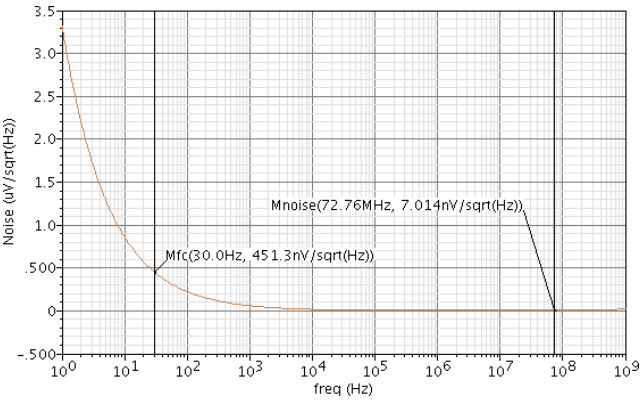

Fig. 8. Noise response: Flicker = 5.3µVrms; Shot Noise = 53µVrms.

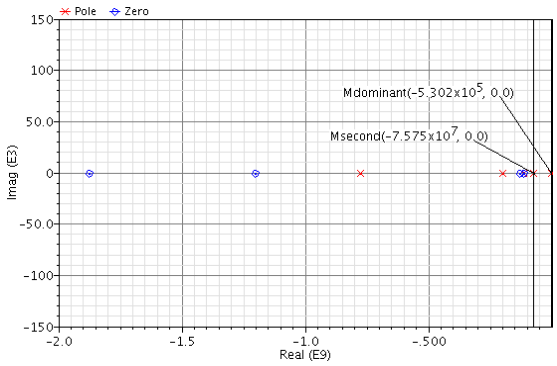

Fig. 9. Pole and Zero locations.

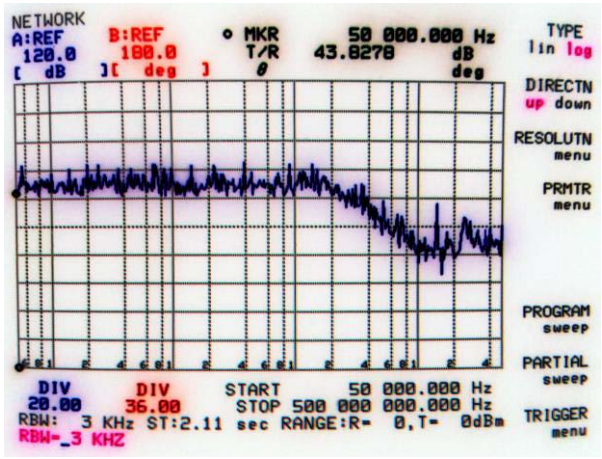

Fig. 10. Measured AC response: Gain of 44 dB; GBW of around 90 MHz.

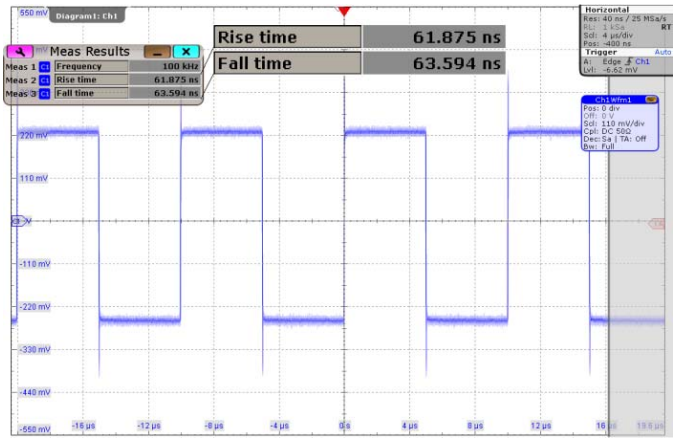

Fig. 11. Step response: Time of rise of 62 ns; Time of fall of 64 ns.

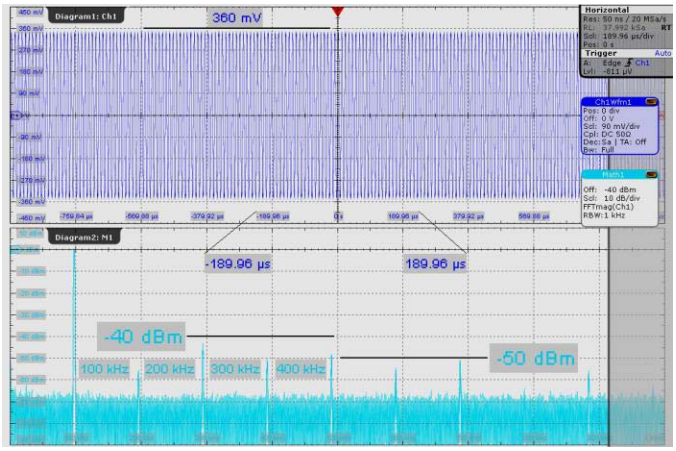

Fig. 12. Measured response to a 100 kHz and 600mVpp sinusoidal input with Blackman-Harris window coherent sampling for harmonic distortion.

are shown in Figs. 7–9, indicating stability, with a dominant pole around 530 kHz and a low noise contribution at GBW. A simulated PSRR of 99.3 dB and a simulated CMRR of 124.4 dB have been achieved in this specific solution, remarkably surpassing [6] and [7]. The fabricated prototype measurement follows the procedure described in [6] and [7]. The gain Bode plot is shown in Fig. 10, while the step response is shown in Fig. 11, demonstrating rise and fall times of approximately 62 and 64 ns, respectively, in line with a lower GBW, when compared to [6] and [7]. The FFT of an output sine wave in unitary gain configuration is shown in Fig. 12, where it is possible to depict a third harmonic roughly 45 dB lower than the fundamental, following the achieved gain of about 44 dB. A systematic offset voltage of approximately 2 mV is measured with an OS of 80% of V_{DD}, following the procedure in [7]. An exploration in depth, to verify the possibility of using this topology in a secure way when operating at lower voltages, has been carried out using AIDA, resulting in FOMs better than 1300 and 1100 MHz × pF/mW for supplies of 1.1 V and 0.9 V correspondingly, as presented in Fig. 13. Table II positions the solution among important single-stage amplifiers in recent literature, showing the attractiveness

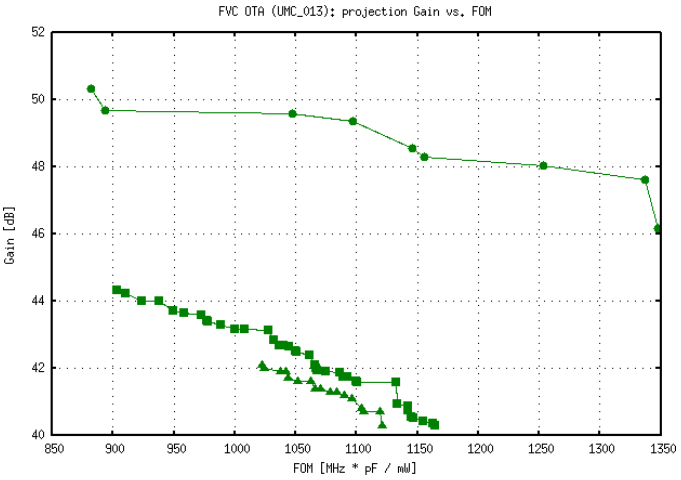

Fig. 13. Low-voltage POFs in typical conditions: • 1.1V; ■ 1.0V; ▲ 0.9V.

TABLE II
COMPARISON WITH RECENTLY PUBLISHED SINGLE-STAGE OTAS

Work	I_{DD} [mA]	Gain [dB]	GBW [MHz]	Load [pF]	PM [°]	FOM [MHz×pF/mW]	Tech [nm]	Supply [V]	Year	Available OS
[6][1]	1.00	47.0	170.6	6.0	55	310.3	130	3.3	2017	OS ≈ V_{DD} - 2×VDS_{SAT}
[7][1]	1.10	58.0	202	6.0	50	333.9	130	3.3	2017	OS ≈ V_{DD} - 2×VDS_{SAT}
[12][1]	0.80	60.9	134.2	5.6	71	521.9	180	1.8	2009	OS ≈ V_{DD} - 4×VDS_{SAT}
[13][2]	1.00	85.6	987.0	1.0	67	548.3	180	1.8	2015	OS ≈ V_{DD} - 4×VDS_{SAT}
[14][2]	0.09	84.0	12.5	1.0	81	138.9	180	1.0	2013	OS ≈ V_{DD} - 4×VDS_{SAT}
[15][2]	3.67	94.9	414.0	2.0	82	75.2	130	3.0	2011	OS ≈ V_{DD} - 4×VDS_{SAT}
[16][2]	5.00	91.5	714.5	7.5	62	595.3	130	1.8	2012	OS ≈ V_{DD} - 4×VDS_{SAT}
[17][2]	2.17	67.0	920.0	0.5	67	117.2	180	1.8	2011	OS ≈ V_{DD} - 2×VDS_{SAT}
[18][2]	0.65	72.0	159.0	2.2	70	595.9	180	0.9	2007	OS ≈ V_{DD} - 4×VDS_{SAT}
[19][2]	0.26	70.2	83.0	7.0	70	1862.2	130	1.2	2010	OS ≈ V_{DD} - 4×VDS_{SAT}
This work[1]	**0.32**	**44**	**80**	**6.0**	**55**	**1363.6**	**130**	**1.2**	**2019**	**OS ≈ V_{DD} - 2×VDS_{SAT}**

[1]Experimental measurements, [2]Simulation results

of both the proposed new amplifier topology and the framework, that covers the full design and optimization processes, with XRC results. This brief is the second best, regarding the FOM, with a drained power under 0.4 mW while achieving an almost rail-to-rail OS.

Through Table II, it is possible to acknowledge the important advantages of the proposed work, when compared to related recent literature, i.e., an experimentally measured high level of energy-efficiency, together with a high output-swing, being suitable to operate properly under lower voltage supplies, i.e., down to 0.9 V.

V. CONCLUSION

This brief presented the final step towards a complete new family of single-stage OTAs of high energy-efficiency with an innovative gain improvement strategy, in a way that is free from the traditional cascode implementations. The design of an OTA biased by a fully-differential folded VC doublet was fully-automated, from sizing to layout, using AIDA framework. Measurement results confirmed that a gain of approximately 44 dB can be achieved, together with a FOM higher than 1300 MHz × pF/mW. The circuit is able to operate properly under a 0.9 V voltage supply with proper DC biasing, meeting all the performance and functional constraints.

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