

Fault Detection and Diagnosis Technique for a SRM Drive Based on a Multilevel Converter Using a Machine Learning Approach

Tito G. Amaral^{1,*}, V. Pires¹, Daniel Foito^{1,2}, A. J. Pires^{1,2}, J. F. Martins^{2,3}

¹ESTSetúbal, Instituto Politécnico de Setúbal, Setúbal, Portugal

²CTS – Uninova, Lisbon, Portugal,

³DEEC/FCT/UNL, Lisbon, Portugal

* tito.amaral@estsetubal.ips.pt; vitor.pires@estsetubal.ips.pt; daniel.foito@estsetubal.ips.pt; armando.pires@estsetubal.ips.pt; jf.martins@fct.unl.pt

Abstract—SRM drives based on multilevel converters is now a solution well accepted due to their interesting features like extended voltage range and capability to fault tolerance. However, one aspect that is fundamental to ensure fault tolerance or preventive maintenance is the fault detection and diagnosis of failures in power semiconductors. In this way, in this paper it is presented a new diagnostic method for the failure of those semiconductors in asymmetric neutral point clamped converters. The proposed method will be based on the development of specific patterns that are associated to each semiconductor and fault type. The procedures presented here are based on the image identification of the currents patterns in the multilevel converter that allow the identification of distinct fault type. The pattern recognition system uses visual-based efficient invariants features for continuous monitoring of multilevel converter. The proposed method will be verified through several tests in which were used a simulation tool and an experimental prototype.

Index Terms—Fault Diagnosis, Detection, pattern recognition, machine learning, SRM, multilevel converters.

I. INTRODUCTION

One of the electrical machines that was adopted due to their interesting characteristics is the Switched Reluctance Machine (SRM). In fact, this machine presents interesting features, especially due to the inexistence of the magnets, simple design and robustness [1,2]. As a result, their adoption in many applications, such as, electric vehicles [xx], aeronautics, renewable generators, pumping systems, among others [2-6], was something natural. However, this machine requires a driver, although this is something natural in other machines for many applications.

There are several power converter topologies that have been proposed and used for the SRM driver. The first ones are based in a two voltage level structure and with an asymmetric configuration. This is the case for example of the two-level asymmetric half bridge converter (AHBC). However, many other topologies with a two voltage level

structure have been used, as can be seen in review works [7-9]. However, as an alternative to these topologies, multilevel converters have also been proposed since they allow to provide higher torque range, but also, usually some fault tolerance to switch faults [10]. Several different topologies were proposed, some with higher switch number and others with lower [11-14]. However, the ones with lower count switch usually are very limited regarding fault tolerant capability. In this way, the most adopted taking into consideration this feature are the ones based on the classic inverter multilevel characteristics, such as, asymmetric NPC half bridge converter. However, there are some particular faults that this converter presents some limitation. Thus, to overcome these limitations a full NPC bridge converter was proposed [15]. Anyway, this NPC structure is very interesting since allows to operate the converter under a short-circuit fault of the switch without the introduction of fuses or static or mechanical switches.

One fundamental aspect associated to the fault tolerance operation of the converter, is the fault detection and diagnosis of the switch(s) under fault. In this way, several methods have been proposed. Most of them have been focused on the two-level converters [16-19]. However, due to the capability of the multilevel converter to operate in fault tolerant condition, the detection and diagnosis of the fault in this kind of topologies is very important. However, only now started to appear fault detection and diagnosis for this kind of topologies [20]. Anyway, many works is still required in these algorithms regarding the multilevel converters.

Due to the importance in the study and development of fault detection and diagnosis algorithms for the multilevel converters used in the SRM drives, this paper proposes a new approach. This new approach is based on the identification of specific machine current patterns, by which, a proposal to create them is presented. The algorithm is able to detect not only the switch under fault, but also the type of fault that is associated, i.e., open or short-circuit. The specificities and capability of the

proposed approach will be verified by several simulation tests.

II. CONFIGURATION AND OPERATION OF THE SRM DRIVE

As referred in the previous section, besides the higher torque range, SRM drives based on multilevel topologies also presents some fault tolerance capability. This is the case of the asymmetric NPC half bridge converter, showed in Fig. 1. Since these converter uses more transistors, under a fault in one or more of them is possible to still operate the machine. On the other hand, due to the fact that uses two switches in serial connection, a short-circuit fault in one of them, will not affect the demagnetization of the machine windings.

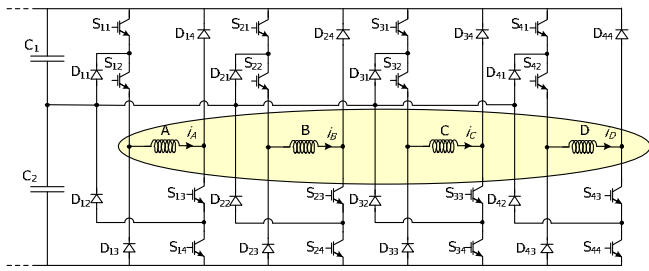


Fig. 1. Power converter used in the SRM drive based on the NPC Asymmetric-Half-Bridge.

The topology presented in Fig. 1, has anyway some limitation. One of the limitations is when there is an open switch fault in the inner switches. In this case, it is not possible to apply a positive voltage to the machine winding by which their magnetization is not anymore possible. However, this can be overcome with the full-bridge NPC converter as shown in Fig. 2 [xx]. However, in normal mode the switches that operate are the same as the ones presented in the topology of Fig. 1 by which under the point of view of fault identification is the same.

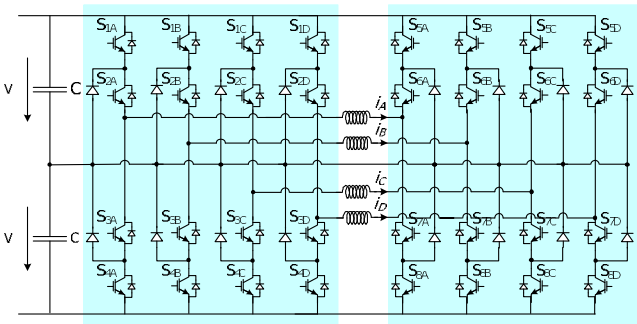


Fig. 1. Power converter used in the SRM drive based on the NPC Asymmetric-Half-Bridge.

These converters allow applying to each of the SRM winding several voltage levels. Each of the voltage levels is function of the switches combination. In table I is possible to see the applied voltage levels to SRM winding A function of the switches combination for the topology presented in Fig. 1. This table also shows that for some

voltage levels there are redundant switches combinations.

TABLE I. Applied voltage levels to SRM winding A function of the switches combination for the topology presented in Fig. 1.

Operation mode	Switches ON	Voltage level
1	$S_{11}, S_{12}, S_{13}, S_{14}$	$+V_{C1} + V_{C2}$
2	S_{11}, S_{12}, S_{13}	$+V_{C1}$
3	S_{11}, S_{12}, S_{14}	$+V_{C2}$
4	S_{11}, S_{12}	0
5	S_{13}, S_{14}	0
6	S_{12}	$-V_{C1}$
7	S_{13}	$-V_{C2}$
8	-	$-V_{C1} - V_{C2}$

There are different fault types that can appear in the multilevel converter power semiconductors, namely open switch fault or short-circuit fault. Depending on the fault, it can affect differently the operation of the SRM. For example an open switch fault could affect the magnetization of the machine windings while the short-circuit the demagnetization. On the other hand, in the case of the first topology, there is a specific fault the severely affects the machine operation, namely when there is an open-fault in switches S_{12} or S_{13} . In the case, it is not possible to magnetize the SRM winding. This problem could be solved with the topology presented in Fig. 2. Thus, or only to warn about a power semiconductor fault or to allow for a fault tolerant operation, the detection and diagnosis of faults are fundamental.

III. PROPOSED FAULT DETECTION AND DIAGNOSIS APPROACH BASED ON MACHINE LEARNING

The 4D current trajectory can be used to identify the faulty switch since typical patterns are obtained. The proposed approach is converted into a pattern recognition analysis. Fig. 3 shows the proposed three step algorithm for the fault detection and diagnosis of the multilevel converter. The inputs for the machine learning based system are the currents in the converter ($i_A, i_B, i_C, i_D, i_{m1}, i_{m2}, i_{m3}, i_{m4}$) and the output is the identification of the converter working condition.

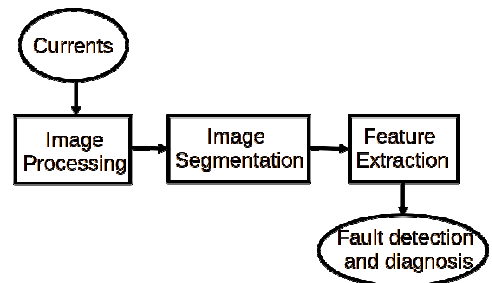


Fig. 3. Structure of the fault detection and diagnosis based on machine learning.

In the image processing stage the four currents vector [i_A, i_B, i_C, i_D] is transformed into a binary image contour. This procedure is obtained by 1D to 2D signal transformation of the currents followed by the image composition where each sample of the current vector

pattern will be considered as a binary pixel in an image [21]. All current vector samples $[i_A, i_B, i_C, i_D]$ generate points that belong to the contour of a region in the image. The same methodology is used in the four currents vector $[i_{m1}, i_{m2}, i_{m3}, i_{m4}]$ where all samples divide the region into a set of sub-regions where the number and the shape of sub-regions depends on the type of fault converter. In the image segmentations step it is establish the boundary of the region in order to implement the pattern recognition method. The closed region contour is efficiently obtained by computing the coordinates of each point belonging to the segment that links two consecutive vector samples. The last step is the feature extraction which will detect and identify the type of fault. Once a digital image has been segmented, the key features used for fault detection and diagnosis are based on the mass centers of the region and the sub-regions and the number of sub-regions. In order to identify the fault type it will be used the calculation of the region mass center (cmr_x, cmr_y) and the sub-regions mass center $(cmsr_x, cmsr_y)$. The difference between the coordinates of both mass centers, dcm , allows to determine whether there is an open-circuit fault (1).

$$dcm = (cmr_x - cmsr_x) + j(cmr_y - cmsr_y) \quad (1)$$

In order to obtain a diagnostic variable that is independent of the actual load, the proposed methodology will use the equivalent circumference radius, re , as half the length of the major axis of the ellipse that has the same normalized second central moments as the region. The following normalized diagnostic variable NDV is given by:

$$NDV = \frac{dcm}{re} \quad (2)$$

The obtained images for healthy and faulty converters are distinct, and their differences are detected and analyzed in the feature extraction step.

IV. RESULTS

The proposed approach was tested by computer simulations and using a laboratory prototype. The simulations results were carried out on a 2.00 GHz Intel Core i7-1280P CPU with 16 GB RAM using the Matlab/Simulink simulation tool. In order to validate the proposed approach, several simulations results of the multilevel converter with and without fault were obtained.

The first test was for the case where there is no switch fault in semiconductor. Fig. 4 shows the motor currents of the multilevel converter. The correspondent representation of the currents i_A, i_B, i_C and i_D in orthogonal view are in Fig.5.

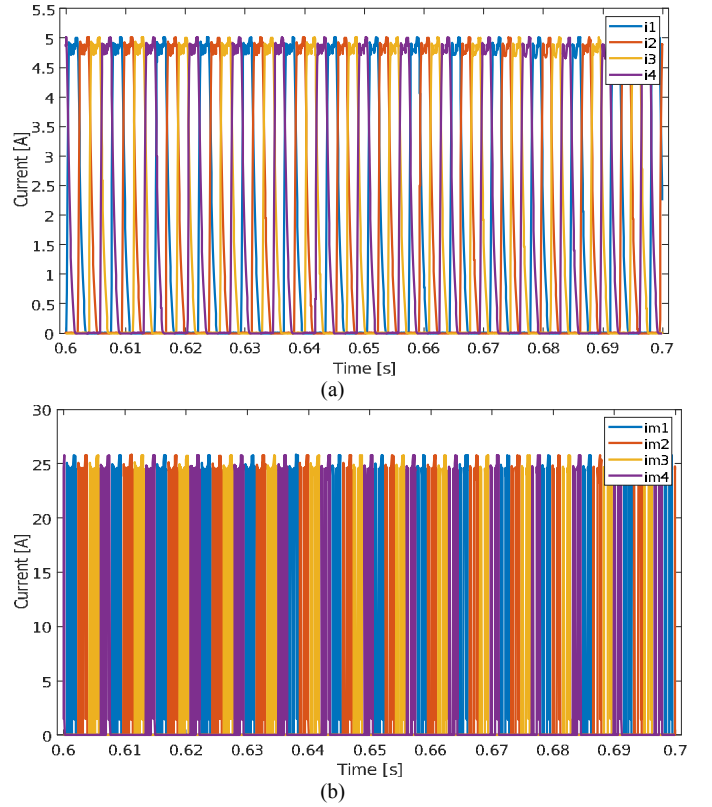


Fig. 4. Results of a test without any fault (a) four motor currents (b) Im currents.

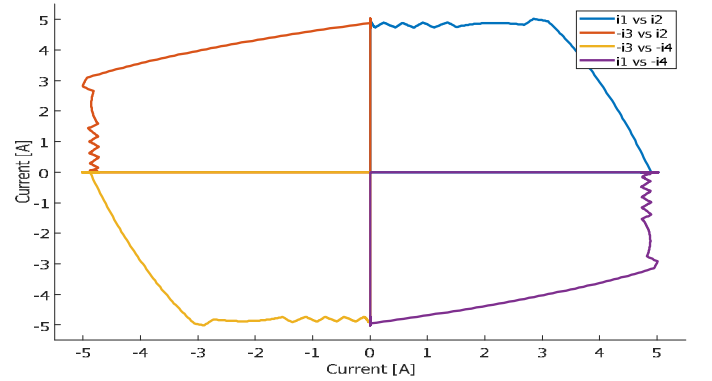
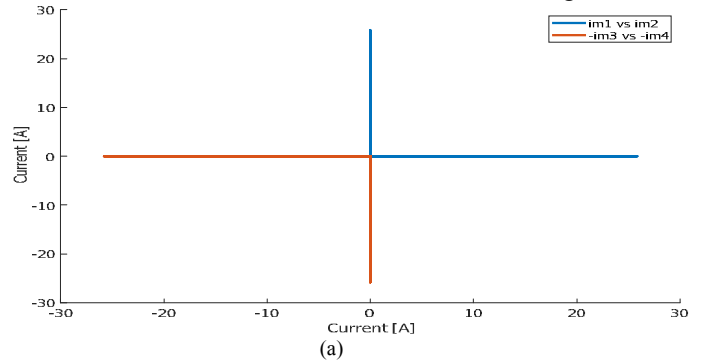


Fig. 5. Four currents representation in orthogonal view without any fault.

The representation of the currents i_{m1}, i_{m2}, i_{m3} and i_{m4} in orthogonal view are in Fig.6. It can be seen that in both figures their representation is identical, thus using only one of these representations to create the sub regions. Fig.7 shows the outer contour of the region generated by the currents i_A, i_B, i_C and i_D and the four created sub-regions.



(a)

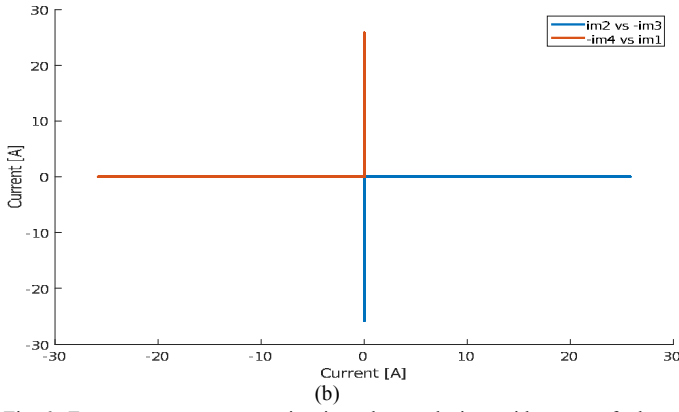


Fig. 6. Four currents representation in orthogonal view without any fault. (a) i_{m1} vs i_{m2} and $-i_{m3}$ vs $-i_{m4}$ (b) i_{m2} vs $-i_{m3}$ and $-i_{m4}$ vs i_{m1}

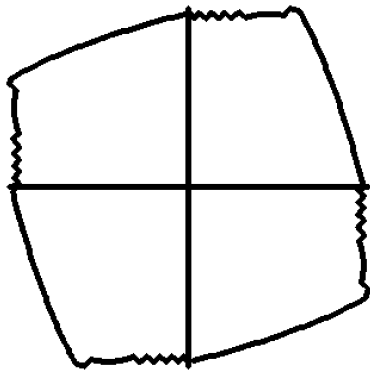


Fig. 7. Contours of the regions in healthy motor condition.

The second test was performed for the open switch fault of the semiconductor S_{21} . The obtained new results can be seen in Fig.10 where it is possible to verify the current in the winding is associated with the leg under fault. Fig.11 shows the correspondent representation of the currents i_A , i_B , i_C and i_D in orthogonal view.

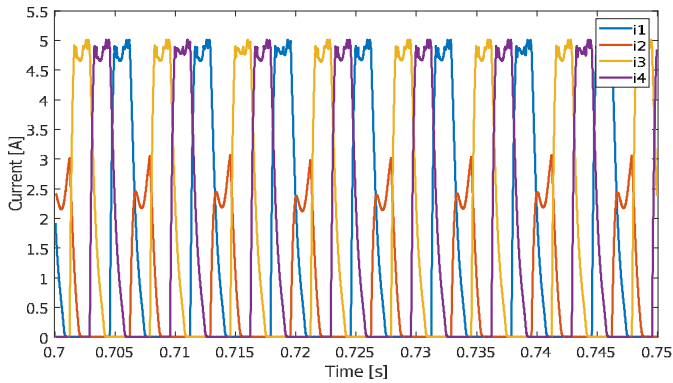


Fig. 10. Motor currents of a test for an open switch fault in S_{21} .

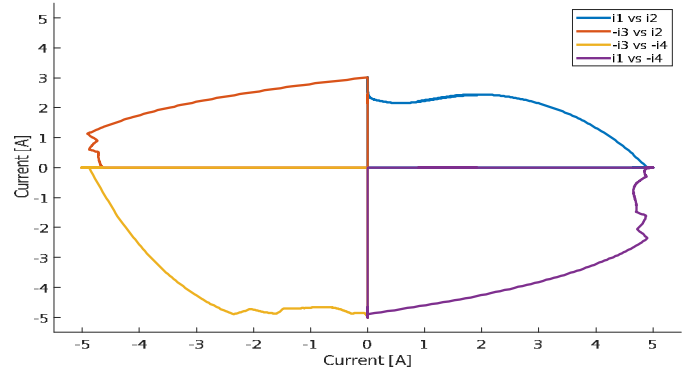


Fig. 11. Four currents representation in orthogonal view for an open switch fault in S_{21} .

The outer contour of the region generated by the currents i_A , i_B , i_C and i_D and the four created sub-regions are shown in Fig.12. In Fig.13 is presented the position of the region mass center and the sub-regions mass center. In the open switch fault condition the centers of mass doesn't and then the normalized diagnostic variable is different from zero.

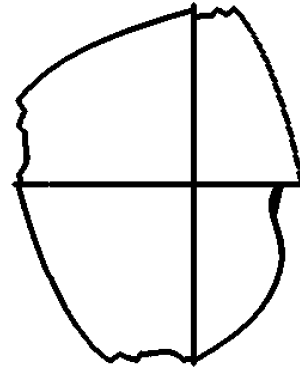


Fig. 12. Contours of the regions for an open switch fault.

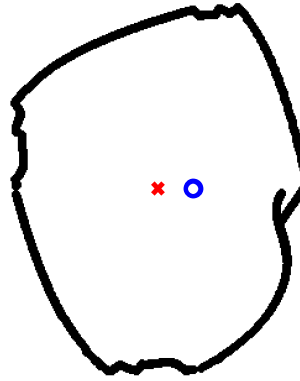


Fig. 13. Position of centers of mass for an open switch fault.

Another test, in which a different fault type was considered, was also implemented. In this case, a short-circuit fault of the semiconductor S_{11} was considered. The obtained results can be seen in Fig.15 where it is possible to verify the i_m current associated with the leg under fault. The correspondent representation of the currents i_A , i_B , i_C and i_D in orthogonal view are in Fig.16. The representation of the currents i_{m1} , i_{m2} , i_{m3} and i_{m4} in orthogonal view are in Fig.17. It can be seen that although the figures are not identical both divide the region into 3 sub regions. In the same way as happens in the previous situation it is used one of these representations to create the sub regions.

Fig.18 shows the outer contour of the region generated by the currents i_A , i_B , i_C and i_D and the four created sub-regions.

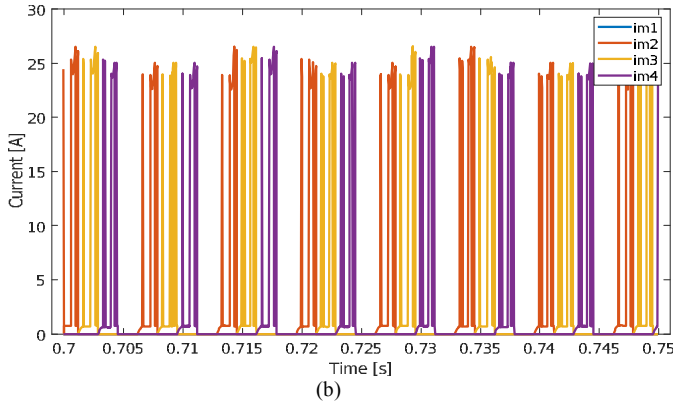
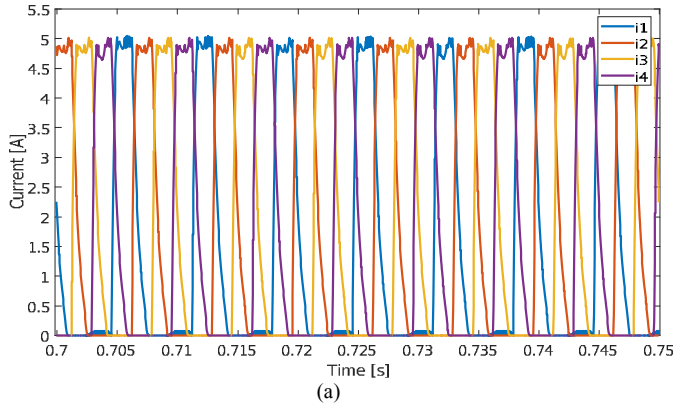


Fig. 15. Results of a test for a short-circuit fault in S_{II} (a) four motor currents (b) short-circuit Im currents.

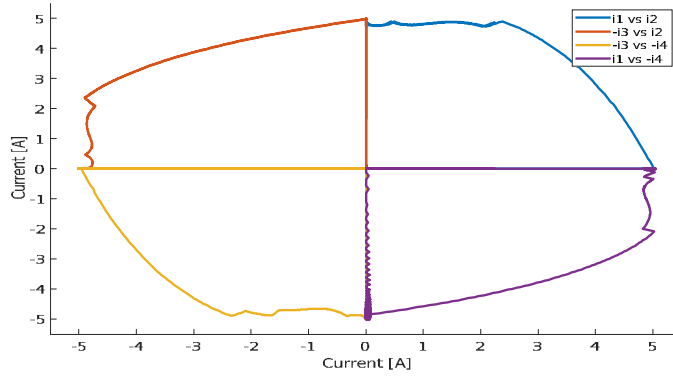


Fig. 16. Four currents representation in orthogonal view for a short-circuit fault in S_{II} .

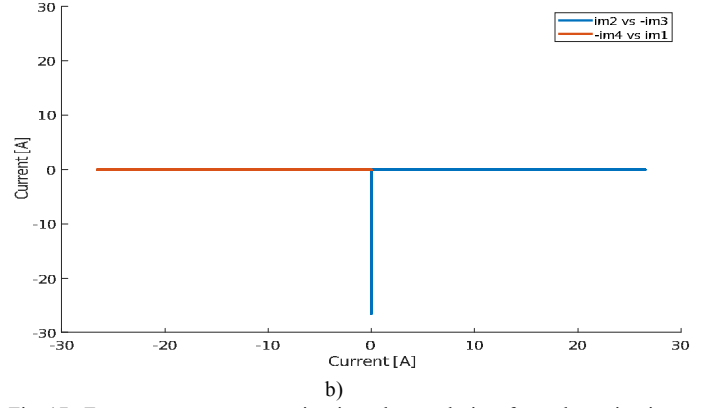
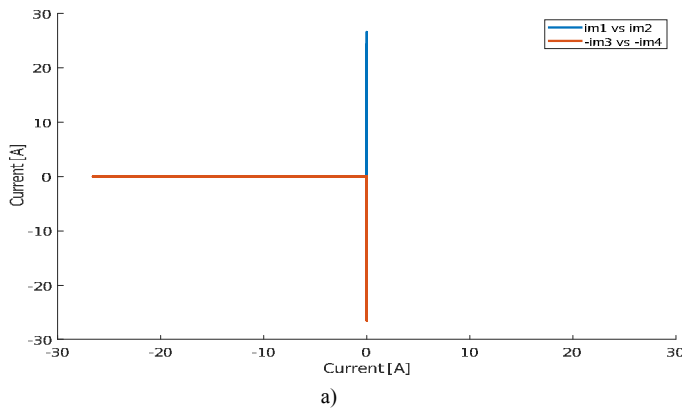


Fig. 17. Four currents representation in orthogonal view for a short-circuit fault in S_{II} (a) im1 vs im2 and $-im3$ vs $-im4$ (b) im2 vs im3 and $-im4$ vs im1.

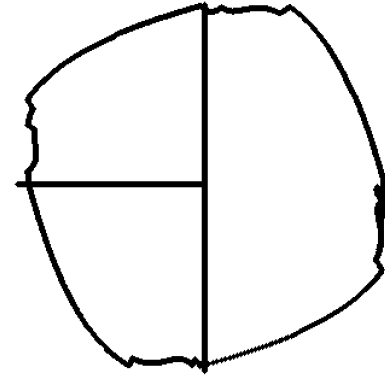


Fig. 18. Contours of the regions for a short-circuit fault.

V. CONCLUSIONS

Due to the importance on the detection and diagnosis a switch fault in a SRM drive with a multilevel converter, a new approach was presented in this work. This new approach was based on the recognition of specific patterns that can be obtained from the SRM currents. In this way, it was also proposed a way to create those patterns that will differ taking into consideration the switch and fault type. The approach was based on the current signals, and is independent of the operation mode. Fault detection and diagnosis based on simulation results were presented. The results showed the extracted features have different values depending of the fault type and the switch under fault. This makes possible to detect and identified the switch and the correspondent fault type.

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