Study of the HVDC Dual Transmission System Under Faults in the Power Converters

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***Abstract*— HVDC transmission systems based on voltage source converters have lately emerged as a good alternative to conventional AC transmission. In these transmission systems multilevel converters have become a promising energy conversion technology. The reliability of the power converters are extremely important since a fault in these equipments may lead to an unavailability for a long period of the transmission system. Thus, this paper will focuses in HVDC dual transmission system under semiconductor failure conditions. As presented in this paper this structure presents interesting characteristics under the point of view the reliability considering a power semiconductor failure. It will present the consequences for the transmission system when there is a semiconductor fault. A study for the change of the modulation system in order to ensure DC link capacitors voltage balance under a fault condition is also presented. Simulation studies are shown in order to confirm the characteristics of the proposed methodology in normal and fault condition mode.**

Keywords— HVDC transmission; Multilevel converter, Dual converter; Vectorial modulator; Semiconductor fault conditions.

I. INTRODUCTION

The HVDC transmission system has emerged as an attractive alternative to traditional AC transmission, due to its capability of transmitting large quantities of power over long distances. Also, can be seen as a useful solution to other problems of transport networks, such as network congestion, stabilization of power flows in integrated power systems and asynchronous connections of AC power systems [1-2].

At their beginning, HVDC transmission systems were based on current source converters (CSC) with line commuted thyristor, so called line commuted converters (LCC). This technology allowed that large amounts of power could be processed, however without full controllability of the system and with high harmonic contents.

The development and the availability of high rated fully controllable switches, such as the gate turn-off thyristor (GTO) and the insulated gate bipolar transistor (IGBT) contributed to the use of voltage source converter (VCS) as an attractive alternative to the CSC for HVDC systems [3].

In comparison with the classical HVDC systems, the VSC based HVDC offers a series of advantages such as, the ability to create a completely independent AC voltage waveform, the independent control of active and reactive power flow, the improvement of voltage stability and the increase of the transfer capability in AC systems [4-5].

The use of multilevel converters in HVDC systems, can be a suitable solution, to situations where are required higher voltage and power operation capability with lower voltage rating semiconductor devices, lower common-mode voltages, higher efficiency and reduced harmonic distortion is the use of multilevel converters.

In order to reduce the switching frequency, lower dv/dt stresses overall and obtain AC currents with low distortion, topologies of multilevel converter have been studied and proposed. The neutral point clamped (NPC) converter [6-7], the flying capacitor converter [8-9] and the cascaded connection of H-bridge [10] are the most widely known and used topologies. The diode clamped converter provides multiple voltage levels through connection of the phases to a series connected bank of capacitors. This topology offers the advantage of smaller output ripples, total positive or negative supply voltage shared among semiconductors and reduced switching losses. The flying capacitor involves series connection of capacitor clamped switching cells, instead of diodes. This arrangement has more switching redundancies, which can be used to balance the flying capacitors voltage, however needs more capacitors. The cascaded H-bridge converter consists of series power conversion cells to get a sinusoidal voltage output. It combines higher number of output voltage levels with a good harmonic range using low-cost low voltage power semiconductors and capacitors. The modular multilevel converter is another topology that has been proposed and implemented, in order to avoid the drawbacks of conventional VSC in HVDC applications [11-12]. Another multilevel converter topology that can be used in HVDC technology is the dual transmission system, that has recently been introduced [13]. This topology is characterized by a simple structure since uses two standard three-phase voltage source converters.

Due to importance of the reliability of HVDC transmission systems, several studies have been presented. However, most of the studies have been focused on the AC and DC system faults [14-15]. Much less efforts have been made regarding a fault in the power converter switches. Thus, this paper analyses the operation of HVDC transmission systems based on the dual two-level converter topology, in normal and failure conditions of semiconductors. As will be presented, this topology presents interesting characteristics regarding fault tolerant operation under these fault types. It also is presented a study of the vector modulation that will ensure the capacitor voltage equalization for normal and failure conditions.

II. HVDC MULTILEVEL BASED ON DUAL TWO LEVEL CONVERTER

The HVDC transmission system that will be studied is presented in Fig.1. It consists of the two standard three-phase two level voltage source converters connected to AC sides by a three phase transformer with the secondary in the open end configuration. The DC link capacitor provides the necessary DC voltage for the dynamics of the system and offers filtering for the DC harmonics.

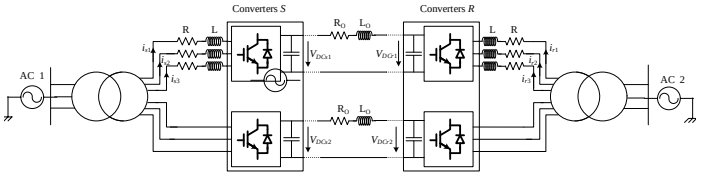

Fig. 1. Diagram configuration of the HVDC based on dual two level converter.

In the dual two-level converter topology (Fig. 2) the several series connected IGBTs are used for each semiconductor to support a high blocking voltage capability and consequently increase the DC bus voltage level of the HVDC system.

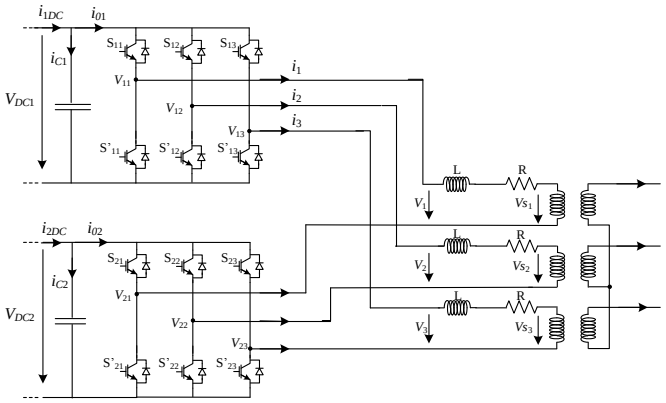

Fig. 2. Circuit diagram of the dual two-level converter.

To obtain the dual converter model, ideal power switches will be considered. So, in accordance with Fig. 2, the time dependent variable $\gamma_k(t)$ with $k \in \{1,2,3\}$ which represents the states of the switches, can be expressed by (1).

$$\gamma_k(t) = \begin{cases} 1 \text{ if } S_{k1} \text{ is ON } \wedge\ S_{k2} \text{ is OFF} \\ 0 \text{ if } S_{k1} \text{ is OFF } \wedge\ S_{k2} \text{ is ON} \end{cases} \qquad (1)$$

The AC output voltages at each of the converters are function of the power semiconductors state and DC voltage sources, as expressed by equation (2).

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} \gamma_{11} \\ \gamma_{12} \\ \gamma_{13} \end{bmatrix} V_{DC1} - \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} \gamma_{21} \\ \gamma_{22} \\ \gamma_{23} \end{bmatrix} V_{DC2} \qquad (2)$$

In the α,β plane, the AC output voltages can be obtained using the Clarke-Concordia matrix transformation, through the following relationship [16]:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \gamma_{11} \\ \gamma_{12} \\ \gamma_{13} \end{bmatrix} V_{DC1} - \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \gamma_{21} \\ \gamma_{22} \\ \gamma_{23} \end{bmatrix} V_{DC2} \qquad (3)$$

From the relation (3) and according to all the switching states, it is possible to verify that 64 different output voltage levels can be obtained. However, bearing in mind that DC voltages of the converters are equal (V_{DC1}=V_{DC2}), it will be achieved 19 different output voltage vectors (Fig. 3). The other vectors are redundant and will be used to capacitor voltage balance.

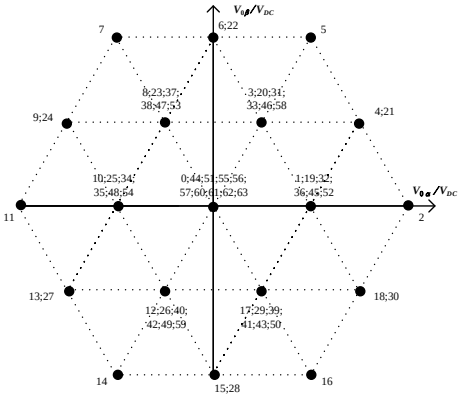

Fig. 3. Output voltage vectors of the three-phase dual two-level converter, in α, β frame.

The state space model of the dual converter in three phase reference frame and *dq* frame, will be necessary to study the HVDC system controller. Then, applying the *dq* transformation and considering V_{DC1}=V_{DC2}=V_{DC}, leads to:

$$\begin{aligned} \frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = &\begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} -\frac{V_{DC}}{L} & 0 \\ 0 & -\frac{V_{DC}}{L} \end{bmatrix} \begin{bmatrix} \gamma_{1d} \\ \gamma_{1q} \end{bmatrix} - \\ &- \begin{bmatrix} -\frac{V_{DC}}{L} & 0 \\ 0 & -\frac{V_{DC}}{L} \end{bmatrix} \begin{bmatrix} \gamma_{2d} \\ \gamma_{2q} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 \\ 0 & -\frac{1}{L} \end{bmatrix} \begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} \end{aligned} \qquad (4)$$

The system controller is developed in order to control the active and reactive power that flows into the HVDC transmission system, as well accomplish the DC link voltage regulation. The active power *P* and reactive power *Q* in *dq* coordinates, can be expressed as:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} V_{sd} & V_{sq} \\ V_{sq} & -V_{sd} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \qquad (5)$$

Whereas that the three phase source voltages are balanced, which means that V_{sq}=0, the following relation can be obtained:

$$\begin{cases} P = V_{sd}\, i_d \\ Q = -V_{sd}\, i_q \end{cases} \qquad (6)$$

The relationship (6) implies that the active power *P* and reactive power *Q*, can be controlled by the control of i_d and i_q respectively, to the reference values i_{dref} and i_{qref}. To control these currents it will be used sliding mode methodology [17].

One of the problems of this structure is the regulation and balance of the voltages in both DC capacitors. This will be made through the use of a voltage vector modulation. Thus, from the analysis of the circuit (Fig. 2) it is possible to verify that from the 64 vectors only 19 define 19 distinct output voltage vectors (Fig. 3). The extra ones are redundant, but will be used to equalize and balance the two DC capacitors voltage. However, the choice of the appropriate voltage vectors implies to know the location of the AC currents. Thus, six sectors will be considered in accordance with Fig. 4. The voltage vectors will be reached through a five level and seven level hysteretic comparators. The outputs of these comparators are the variables $\lambda_\alpha \in \{-2;-1;0;1;2\}$ and $\lambda_\beta \in \{-3;-2;-1;0;1;2;3\}$ corresponding to five and seven selectable levels, respectively. According to this and taking in account the switching combination scheme (Fig. 5), the voltage vector selection will be done using Tables I and II, in accordance with the outputs of the histeretic comparators and the DC capacitor voltage equalization.

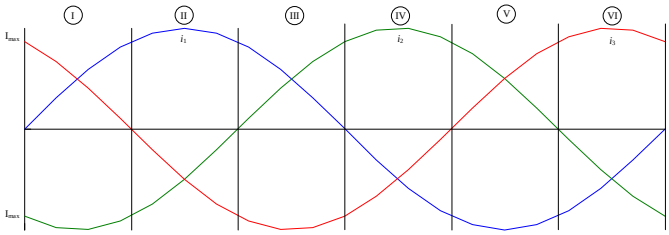

Fig. 4. AC currents and resulting sectors.

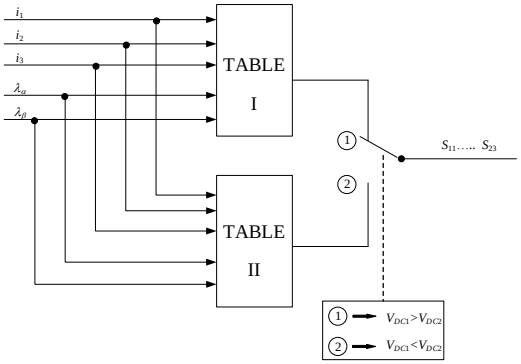

Fig. 5. The switching combination scheme.

TABLE I. WITCHING TABLE FOR $V_{DC1}>V_{DC2}$, SHOWING VECTOR SELECTION UPON THE VARIABLES λ_α AND λ_β.FOR NORMAL OPERATION

	λ_β \ λ_α	**-3**	**-2**	**-1**	**0**	**1**	**2**	**3**
	-2	13	14	14	15	16	16	30
	-1	13	13	12	15	17	30	30
I	**0**	11	34	34	0	1	1	2
	1	24	24	23	22	31	4	4
	2	24	7	7	22	5	5	4
	-2	13	14	14	28	16	16	30
	-1	13	13	42	28	17	18	30
II	**0**	11	25	25	0	32	32	2
	1	9	9	23	22	31	4	4
	2	9	7	7	22	5	5	4
	-2	13	14	14	28	16	16	18
	-1	13	13	26	28	43	18	18
III	**0**	11	25	25	0	32	32	2
	1	9	9	37	22	31	4	4
	2	9	7	7	22	5	5	4
	-2	27	14	14	15	16	16	18
	-1	27	27	26	15	29	18	18
IV	**0**	11	35	35	0	36	36	2
	1	9	9	8	22	31	4	21
	2	9	7	7	22	5	5	21

λ_β \ λ_α		-3	-2	-1	0	1	2	3
	-2	27	14	14	15	16	16	30
	-1	27	27	12	15	29	30	30
V	**0**	11	10	10	0	19	19	2
	1	9	9	8	22	3	21	21
	2	9	7	7	22	5	5	21
	-2	13	14	14	15	16	16	30
	-1	13	13	12	15	41	30	30
VI	**0**	11	10	10	0	19	19	2
	1	24	24	8	6	3	4	4
	2	24	7	7	6	5	5	4

TABLE II. SWITCHING TABLE FOR $V_{DC1}<V_{DC2}$, SHOWING VECTOR SELECTION UPON THE VARIABLES λ_α AND λ_β.FOR NORMAL OPERATION

λ_β \ λ_α		-3	-2	-1	0	1	2	3
	-2	27	14	14	28	16	16	18
	-1	27	27	26	28	19	18	18
I	**0**	11	35	35	0	36	36	2
	1	9	9	8	6	33	21	21
	2	9	7	7	6	21	21	21
	-2	27	14	14	15	16	16	30
	-1	27	27	40	15	29	30	30
II	**0**	11	10	10	0	19	19	2
	1	24	24	8	6	3	21	21
	2	24	7	7	6	5	5	21
	-2	27	14	14	15	16	16	30
	-1	27	27	12	15	41	30	30
III	**0**	11	10	10	0	19	19	2
	1	24	24	23	6	20	21	21
	2	24	7	7	6	5	5	21
	-2	13	14	14	28	16	16	30
	-1	13	13	12	28	17	30	30
IV	**0**	11	34	34	0	1	1	2
	1	24	24	23	6	20	21	4
	2	24	7	7	6	5	5	4
	-2	13	14	14	28	16	16	18
	-1	13	13	42	28	17	18	18
V	**0**	11	25	25	0	32	32	2
	1	24	24	23	6	31	4	4
	2	24	7	7	6	5	5	4
	-2	27	14	14	28	16	16	18
	-1	27	27	26	28	43	18	18
VI	**0**	11	25	10	0	32	32	2
	1	9	38	8	22	31	21	21
	2	9	7	7	22	5	5	21

III. HVDC IN FAULT CONDITIONS

Compared with conventional HVDC technology, the HVDC system based on dual two level converter, can operate with accuracy in fault conditions, due to the configuration of the converter. There are several redundant switching combinations for the same output voltage that can be chosen for fault operation. This can be verified making an open switch fault in one of the converters. As an example it will be presented the impact of the S_{11} open switch fault. In this situation [18-20] voltage vectors are not available anymore. Fig. 6 shows the voltage vectors inside a red circle that become unavailable in this fault type.

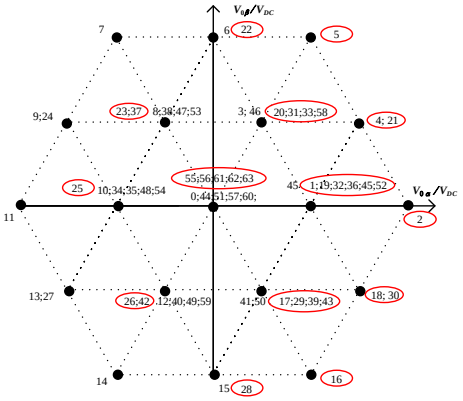

Fig. 6. Output voltage vectors of the dual converter with S_{11} in fault condition.

Since several unavailable voltage vectors were used in the modulation strategy for the normal condition (tables I and II), a change in the choice of the vectors should be made. As an example, it will be presented the impact on the tables related with sector I. In this case the new vectors that must be chosen are presented in tables III and IV.

TABLE III. SWITCHING TABLE FOR $V_{DC1}>V_{DC2}$, SHOWING VECTOR SELECTION UPON THE VARIABLES λ_α AND λ_β.FOR OPEN SWITCH S_{11}.

λ_β \ λ_α	**-3**	**-2**	**-1**	**0**	**1**	**2**	**3**
-2	13	14	14	15	15	15	50
-1	13	13	12	15	50	50	50
0	11	34	34	0	45	45	45
1	24	24	47	6	46	46	46
2	24	7	7	6	6	6	46

TABLE IV. SWITCHING TABLE FOR $V_{DC1}<V_{DC2}$, SHOWING VECTOR SELECTION UPON THE VARIABLES λ_α AND λ_β. FOR OPEN SWITCH S_{11}.

λ_β \ λ_α	**-3**	**-2**	**-1**	**0**	**1**	**2**	**3**
-2	27	14	14	15	15	15	41
-1	27	27	40	15	41	41	41
0	11	35	35	0	45	45	45
1	9	9	8	6	3	3	3
2	9	7	7	6	6	6	3

IV. RESULTS IN NORMAL AND FAULT CONDITIONS

The proposed HVDC structure based on dual two level converter and their control system, in normal and faulty operation, have been carried out by several simulations using the software Matlab/Simuling/Power System Blockset. The presented results were obtained with the HVDC system connected to a grid through two power transformers (132/78.5 kV, 110/78.5 kV) with 70 MVA each.

In order to verify the characteristics of the HVDC system, several simulations were performed. In these tests, firstly the converters are in normal operation, following by a power semiconductor fault. A first test was performed with an open switch fault of converter *S* (switch S_{11}), at 3s. The three-phase AC currents are presented in Fig. 7. From this figure it is possible to verify that the AC currents are balanced and with lower distortion, even after the fault. In fact, from this result is possible to verify that practically there is no impact on the current after the fault. Figs.8 and 9 show the time behavior of DC voltage capacitors in the converters *S* of the HVDC system, before and after the open switch fault S_{11}. From these figures it is possible to verify that the voltage balancing is achieved for both capacitors even after the fault. After the fault there is some impact on the ripple of the voltage. This is due to the lack of some voltage vectors that disappear after the fault. As well, this failure did not have consequences in the balance of the DC capacitor voltages in the converters *R* as shown in Figs. 10 and 9. In this case the voltage ripple is not changed after the fault since in these converters there is no fault.

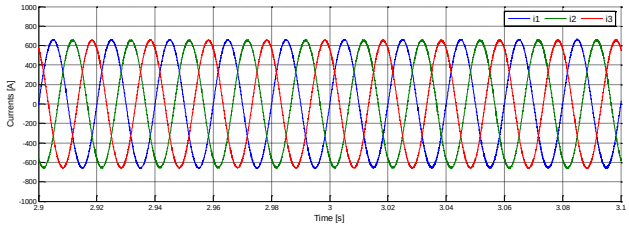

Fig. 7. Three-phase AC line currents of the HVDC converter *S*.

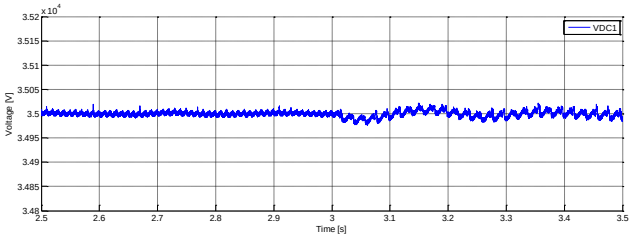

Fig. 8. Voltage waveform of capacitor V_{DC1} of the HVDC converter *S*.

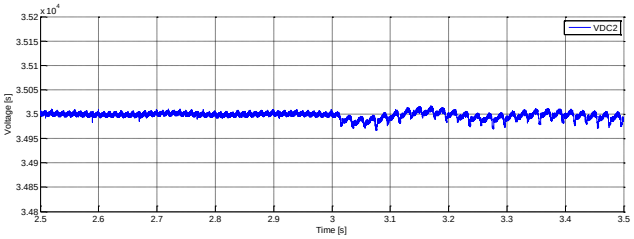

Fig. 9. Voltage waveform of capacitor V_{DC2} of the HVDC converter *S*.

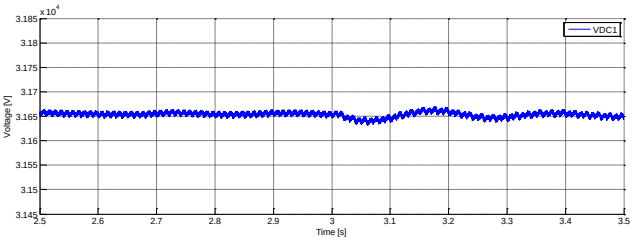

Fig. 10. Voltage waveform of capacitor V_{DC1} of the HVDC converter *R*.

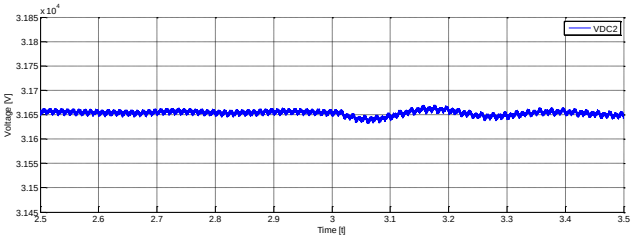

Fig. 11. Voltage waveform of capacitor V_{DC2} of the HVDC converter *R*.

Similar tests to analyze the dynamic response of the HVDC system for an open switch fault in S_{23} of converter *R*, at 3s, was also performed. The time behavior of the three-phase AC currents in converter *R* side related with this test are presented in Fig. 12. From this figure results it is possible to see that the currents remain balanced while presenting very low distortion. Figs. 13 and 14 show that the voltage balance among upper and lower DC capacitors is maintained. After the fault there is an increase of the voltage ripple, but this is expected due to the disappearing of some voltage vectors. The system was also tested for a change of the reference power. In this test was used a reference power with an increase of 30%, and near the nominal power. Fig.15 shows the three-phase AC currents before and after the fault. In this situation, there is an important distortion of the currents after the fault. This is due to the disappearing of some vector voltages with higher amplitude. However, they are nearly balanced and the distortion can be acceptable for this kind of faulty condition. Regarding the DC capacitor voltages, as can be seen from Figs. 16 and 17, after the fault they still maintain the balance, in spite of the fact that the voltage ripple is higher.

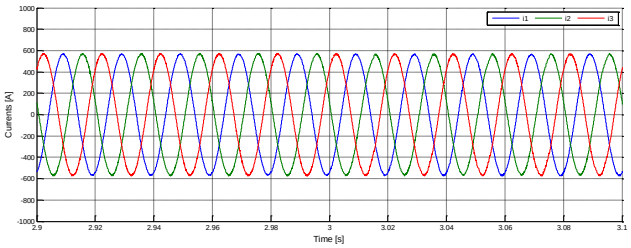

Fig. 12. Three-phase AC line currents of the HVDC converter *R*.

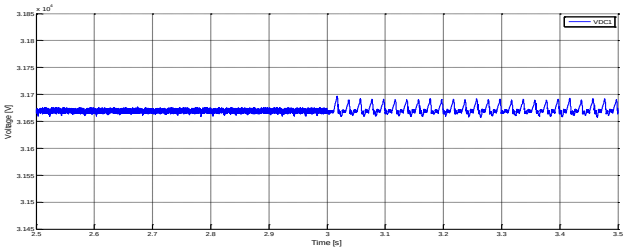

Fig. 13. Voltage waveform of capacitor V_{DC1} of the HVDC converter *R*.

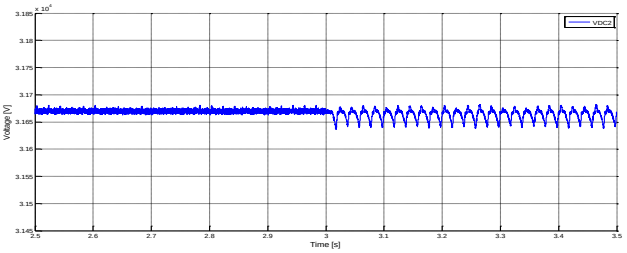

Fig. 14. Voltage waveform of capacitor V_{DC2} of the HVDC converter *R*.

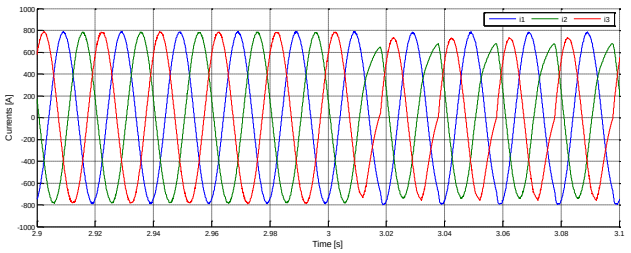

Fig. 15. Three-phase AC line currents of the HVDC converter *R*.

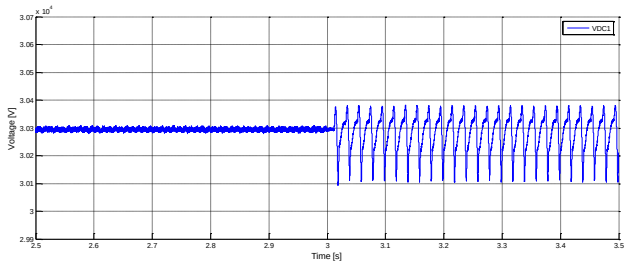

Fig. 16. Voltage waveform of capacitor V_{DC1} of the HVDC converter *R*.

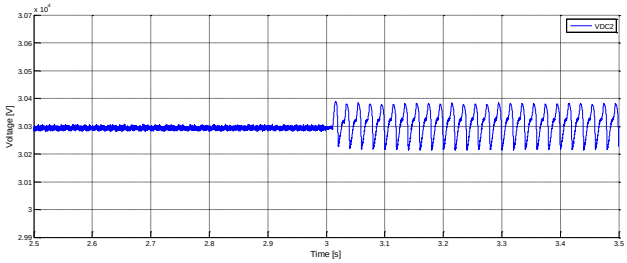

Fig. 17. Voltage waveform of capacitor V_{DC2} of the HVDC converter *R*.

V. CONCLUSIONS

The analysis of a HVDC transmission system based on the dual two-level converter topology under normal and fault conditions operation has been presented. This HVDC transmission system is characterized by two three phase converters with AC terminals connected to a three phase transformer with the open winding configuration. Besides the simple structure this system is characterized by its capability to fault tolerant operation under a semiconductor failure. The system is controlled by a voltage sliding mode controller associated to a vector modulator. It ensures the active and reactive power to their reference values and regulate the DC link of each converter. The vector modulator was designed in order to achieve the balance of the DC capacitors. To reach the fault operation conditions a change of the switching tables used in the vector modulator selection were proposed. This change ensures operation under fault operation conditions, the AC currents maintaining lower distortion and the DC voltage capacitors still keeping their balance. Simulation results have been presented in order to verify the characteristics of the proposed HVDC system under switch fault condition.

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